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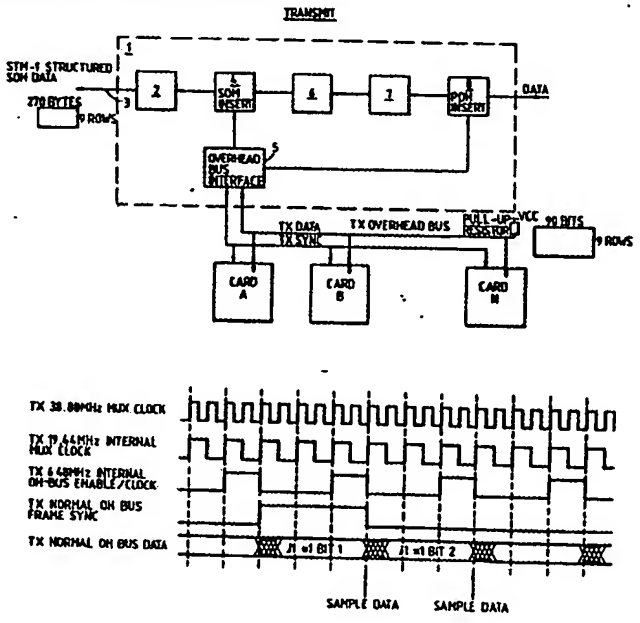
(54) Title: TRANSFER OF SDH OVERHEAD INFORMATION



(57) Abstract

Overhead information is transmitted in a communications system by issuing synchronizing pulses to control an SDH line card. In a frame structure of the system 810 bits of information are organised in 9 rows of 90 bits for transmission at a rate of 8000 bits/second; the information transmitted contains both SOH and path overhead together with spare capacity. The information is presented so that the rising edge of a synchronizing pulse causes the sampling point for data extracted from the bus to be in the centre of the first bit of the frame.

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Transfer of SDH overhead information

This invention relates to a method of transmitting overhead information in a Data Communication System having an SOH frame structure in connection with a pair of MUX terminating equipment in which an overhead bus distributes section and path overhead bytes.

Messages running in the system may be individually clocked at the same nominal rate, however due to jitter and frequency tolerances there may be a lack of synchronisation in the presentation of information within the framework and it is necessary to synchronise all information to ensure that it arrives at the right point in the framework at the correct time and that there is no slippage.

If any slippage does occur it is desirable that an immediate recognition of this takes place and that the necessary alarms are raised so that no transfer of misinformation occurs. The system should also be able to check against false failure signals which may be generated for example by the removal of a card.

In order to achieve the object of dealing with jitter and frequency effects which may vary by as much as 100 ppm, it is possible to set up a system of individual clocks which are wired

separately into the bus. This is not practical in terms of the number of connections which would be required and the number of wires which would be present and it is an object of the present invention to provide a simple and straightforward way of achieving synchronisation.

According to the present invention in a method of transmitting overhead information within a data communications system in which synchronizing pulses control an overhead access card, a frame structure includes a 810 bit arrangement organised in 9 rows of 90 bits which are arranged in use to be transmitted at 8000 frames/second containing SOH and path overhead information as well as some spare capacity. The presentation of information is arranged so that the rising edge of the synchronising pulse causes the sampling point for data extracted from the bus to be in the centre of the first bit of the frame. Subsequent sampling points will slip relative to the data, due to jitter and frequency differences. Since the sampling point is re-phased every frame, no data corruptions occur.

Preferably each row of the SDH frame comprises 270 bytes in length and the section overhead is contained in the first nine bytes. Conveniently the section overhead is contained within the first nine of the twelve bytes in each row of the overhead bus frame.

The system may include a pair of multiplexer cards connected via switching means, the switching means being connected to a plurality of control cards. The system may form part of an optical transmission system. In order to enable the invention to be fully understood one example of a method of transmitting overhead information in a data system in accordance therewith will now be disclosed with reference to the accompanying drawings.

In the drawings Figure 1 shows a schematic layout of SOH distribution in ADMX. Figure 1A is the receive layout and Figure 1B the transmit layout.

Figure 2 is a diagrammatic representation of overhead bus data at the beginning of the frame in this example, and

Figure 3 shows the sequence used for overhead bus data transfer - transmit.

Referring first of all to Figure 1 this shows the general layout in a communication system where information can be transferred either over a fibre optic or an electronic communication system. The system comprises a card 1 which contains a number of functional blocks. The first of these 2 is an STM -1 interface which receives information input over line 3 at the rate of 155 mb/s. From block 1 information is transmitted to block 4 which is the SOH function which operates as insert and extract and passes information between a bus interface 5 as well as through other functions 6, 7 to 8 which is the path overhead function which also inserts and extracts information and exchanges it with block 5. The block 5 outputs onto a bus 9 and is fed variously to the cards (A, B ... N). The information is fed in to line 3 over a fibre optic communication system consisting, in this example, of 270 bytes by 9 rows, of which the first nine of each row are used for control purposes and termed SOH. Referring now to Figure 2, this shows the data structure of the overhead bus. The VCPOH bytes and justification control bits occupy regular byte spaces in line with the SOH bytes.

The first 9 bytes of each row (in an STM-1) are termed the Section Overhead. This contains the Frame Word, pointers, orderwires, parity checks, etc. which must be sourced/terminated on the ADMX. In a drop and insert configuration with 1:1 protection and four STM-1 tributaries it will be possible for the ADMX to receive a maximum of 8 STM-1 signals simultaneously. Under certain conditions it is possible for them all to be plesiochronous. i.e. no longer synchronised. It is a system requirement that the required bytes be correctly terminated, with no loss of data under these conditions. It is also a requirement however to minimise the amount of data storage within the system.

Some of the SOH bytes have defined uses, but the function of the 32 X bytes and the Z1,Z2 bytes are not defined. It is therefore necessary to pass all these bytes to an auxiliary card slot to allow for future developments. This is also true of the

Z3,Z4.Z5 and F2 bytes in each VC3 or VC4 POH.

At the output of the bus interface function 4 of Figure 1 the frame output consists of frames arranged in 9 rows of 90 bits. This gives control over the overhead bus to cards A to N.

It has previously been proposed to distribute the SOH bytes by placing all the bytes from different sources on to a single bus, synchronous with, for example, the Switch clock. The incoming line rates will have a tolerance of +/- 20ppm with respect to the nominal frequency. Since there is no mechanism for justifying the SOH into the frame structure, then byte slips are inevitable.

If the use of the E2 byte as an order wire is considered and if a codec on an Auxiliary card was generating data at the Switch clock rate, to be inserted into the outgoing line, then the E2 may be up to 40 ppm faster than the data rate, producing a byte gap every 25 000 bytes. This may be tolerated in a voice link, although it represents a signal degradation. The effect on the DCC channels will be more significiant however.

The higher capacity DCC occupies SOH bytes D4-E12 and represents a 72 kbyte/sec link. If distributed as above with a maximum 40ppm clock difference:

slip = 72 000 x 40 x 10^-6 = 2.88 bytes/sec

= 1 byte every 0.347 sec

= 0.347 x 72 000 = 1 byte in 25 000

With a message packet length of 128 bytes this represents a message error rate of:

25 000/128 = 1 message in 195 in error, which is unacceptable as it would require frequent packet re-transmission due to errors introduced within the ADMX and is not an acceptable solution to the problem of SOH distribution. Also it should be noted that the function of many of the SOH bytes is unspecified, and future applications may not be able to tolerate this level of errors introduced within the equipment.

It is, thus, necessary that each SOH data source/termination be driven from a clock derived from its

particular STM-1 line rate, if the ADMX is not to introduce errors itself into these channels. This requires a method of distributing the individual timings of up to eight sources around the multiplexer.

Reverting to the SOH distribution within the ADMX as shown, it will be appreciated that a separate highway is provided for each STM-1 source in the system. It should be noted that the quantity of highways may be different from a configuration when differing market requirements pertain.

The simplest method of distributing the Overhead bytes would be to use a six wire bus for each path, with data, frame sync, and clock for receive and transmit. The disadvantage with this approach is the high number of interconnections on the backplane, and more importantly, the number of pins required on control and auxiliary cards. For this reason the invention requires a distribution scheme using only four wire buses.

Each of the overhead distribution highways consists of four wires: Tx-data, Tx-frame-sync, Rx-data and Rx-frame-sync. The proposed data rate is 6.48Mbit/s, which may be conveniently derived from 19.44Mbit/s by dividing by 3 and has the required bandwidth. The individual cards will extract and insert individual bytes on to the highways as required.

The clocks are not required to be distributed because of the close +/-20ppm tolerance between the line rates and other system clocks. The receive data is sent from each mux/optics card with a clock derived from its respective line rate, along with a start-of-frame sync pulse. The other cards may then asynchronously sample the data using a clock derived from another 19.44Mbit/s source, such as the Switch clock. If the phase of the sampling clock is realigned with each frame sync, then no data slips will occur.

Slip rate per frame = bit rate x fractional slip x 1/frame rate
= 6.48x10^6 x 40 x 10^-6 x 1/8000
= 0.0324 bits per frame.
= 11.7 degrees

Assuming jitter on incoming line of 1.5 UI max at 8kHz:

Jitter on bus = 1.5 x 155/6.48

= 0.0625 UI x 360

= 22.5 degrees

Worst-case maximum phase shift per frame = 34.2 degrees.

In the Transmit direction all the cards inserting data on to the highways must do so using a clock derived from a single source, to enable the bytes to be aligned correctly. The transmit sync pulse is at the outgoing line frame rate, and must phase align all interfaces placing data on to the bus.

The frame structure of Figure 2 assumes that the Mux card is partitioned such that the Mux is used to extract both the SOH and POH, which are then distributed together.

The frame structure for each data path as shown in Figure 2 consists of the entire SOH except for row 4 (the pointers), and the frame alignment word A1, A2 bytes and includes the J1, F2 and Z3. Z4. Z5 bytes from the three possible AU3s.

The SOH for each row will be received, buffered, and then transmitted on the distribution bus during one STM-1 row period. This requires only the first nine bytes of storage, due to the bus being synchronised to the line rate. The POH bytes must all be individually buffered however.

Since the VC3/4 POH will move position within the STM-1 frame due to pointer justifications, there may zero, one or two occurrences of a particular byte within a single frame. As Figure 3 shows, the POH must therefore be justified into the SOH distribution frame structure. A single bit is used for the justification control of each POH byte.

Several cards are required to write on to the distribution highways, to insert data into the frame structure. This requires open-collector type bus drivers, with a pull-up resistor, so that all cards can write data. The second criterion is that under failure no card should be able to hold or interrupt the bus and stop the other cards communicating. In this case failure includes

card power loss, card extraction and a diagnosed malfunction, from the system or from the card itself.

The security of the system is important and there are a number of points to be considered in this respect:

a) If a fault is diagnosed on a card then it must not be able to write or hold the bus, and

b) The card designs must ensure that there can be no bus contention due to two cards writing to the same byte within the frame structure. The insertion circuitry should be reset on each frame sync, together with the output clock aligner.

The clock signal operates the frame on the trailing edge of each synchronising pulse and ensures that the information is squarely written in the centre of each bit of the frame. The allocation of information within the rows and columns of the frame structure can be altered depending on the individual requirements of any configuration.

In operation all unused and fixed stuff bytes shall be set to all ones. In the Receive direction this is performed by the Mux ASIC. All disparity (DP) bits except DP#1 are also set to one, and DP#1 is used to set disparity with the whole of the previous frame of data.

In the Transmit direction, as show in Figure 4, a number of different OH will all be inserting data on to the same data line. When a parity check is to be performed, valid data must be present at all times. Since certain byte timeslots may not be accessed by any OH, a pull-up resistor will be required on each Transmit data line , to ensure that all bits are defined, at the input to the Mux.

In the Receive direction, the Mux will generate a disparity bit for each frame of data. i.e. the frame, plus the additional bit, will have odd parity. The parity bit is then inserted in the DP#1 location, in the following frame. Each OH ASIC will be required to perform a similar process and generate a disparity bit for each complete frame of received data. It will

monitor the whole frame for this purpose, even if only accessing a fraction of the data. The calculated value will then be compared with the extracted DP#1 value from the following frame and if they are not equal a failure will be flagged. A three frame persistence check in bytes 10, 11 and 12 of the frames performed on this failure, before an alarm is raised. Each OH may be individually raise an alarm on OH Bus failure.

In the Transmit direction a similar process will occur, but with each OH using a separate disparity bit. Thus each OH must first be configured as to which disparity bit it should access. When an OH inserts data on to the bus, it must calculate the parity of all bits inserted in each frame. The MUX will then insert a disparity bit in the following frame, such that this bit, plus all the data inserted in the previous frame, form an odd parity.

In the Transmit direction, the Mux performs a function similar to that of the OH in the Receive direction. It will calculate the disparity of the whole received frame and compare it with the values of the DP bits in the following frame. To perform this comparison, all the DP bits must first be exclusive-NORed together to form a composite disparity bit. This is then compared with the calculated value and a failure flagged if they are not identical. A three frame persistence check is again performed before an alarm is raised.

The invention ensures that if three following frames are detected as error free then the alarm is cancelled.

It will be appreciated that the method of the invention enables overhead information to be transferred from one SDH line card to or from another card which minimizes the backplane and logic circuits involved. There is a 33% savings in connections over those which otherwise would be necessary. The data rate of 6480 Kbits is a factor of the system clock (38,880 Khz) and can be obtained by dividing the system clock rate by this. Thus the correspondence between the overhead frame structure and the first 9 rows of the SDH frame structure assists the transfer of data from the SDH frame to or from the overhead frame.

CLAIMS

1. A method of transmitting overhead information within a data communications system in which synchronizing pulses control an overhead access card, a frame structure includes a 810 bit arrangement organised in 9 rows of 90 bits which are arranged in use to be transmitted at 8000 frames/second containing SOH and path overhead information as well as some spare capacity characterised in that the presentation of information is arranged so that the rising edge of the sychronising pulse causes the sampling point for data extracted from the bus to be in the centre of the first bit of the frame.

2. A method as claimed in Claim 1 characterized in that the sampling point is re-phased every frame, so that no data corruptions occur.

3. A method as claimed in Claim 1 or Claim 2, characterised in that the section overhead is contained within the first nine of the twelve bytes in each row of the overhead bus frame.

4. A method as claimed in any preceding claims, characterized in that the system includes a plurality of multiplexer cards connected via switching means, the switching means being connected to a plurality of control cards.

5. A method as claimed in any preceding claim, characterized in that the system forms part of an optical transmission communications system

6. A method as claimed in any preceding claim, characterized in that all unused and fixed bytes are set to ones and in that in the receive direction all disparity bits except the first are also set to ones, the first disparity bit being used to set disparity with the whole of the preceding frame.

7. A method as claimed in Claim 6, characterized in that a Mux generates a disparity bit for each frame so that it has odd parity and in that the parity bit is inserted in the following frame.

8. A method as claimed in Claim 6 or Claim 7, characterized in that each overhead ASIC is arranged to generate a disparity bit for each complete frame of received data.

9. A method as claimed in Claim 8, characterized in that if there is not a parity in three consecutive frames an alarm is raised.

10. A method as claimed in Claim 9, characterized in that if three following frames are detected as error free the alarm is cancelled.

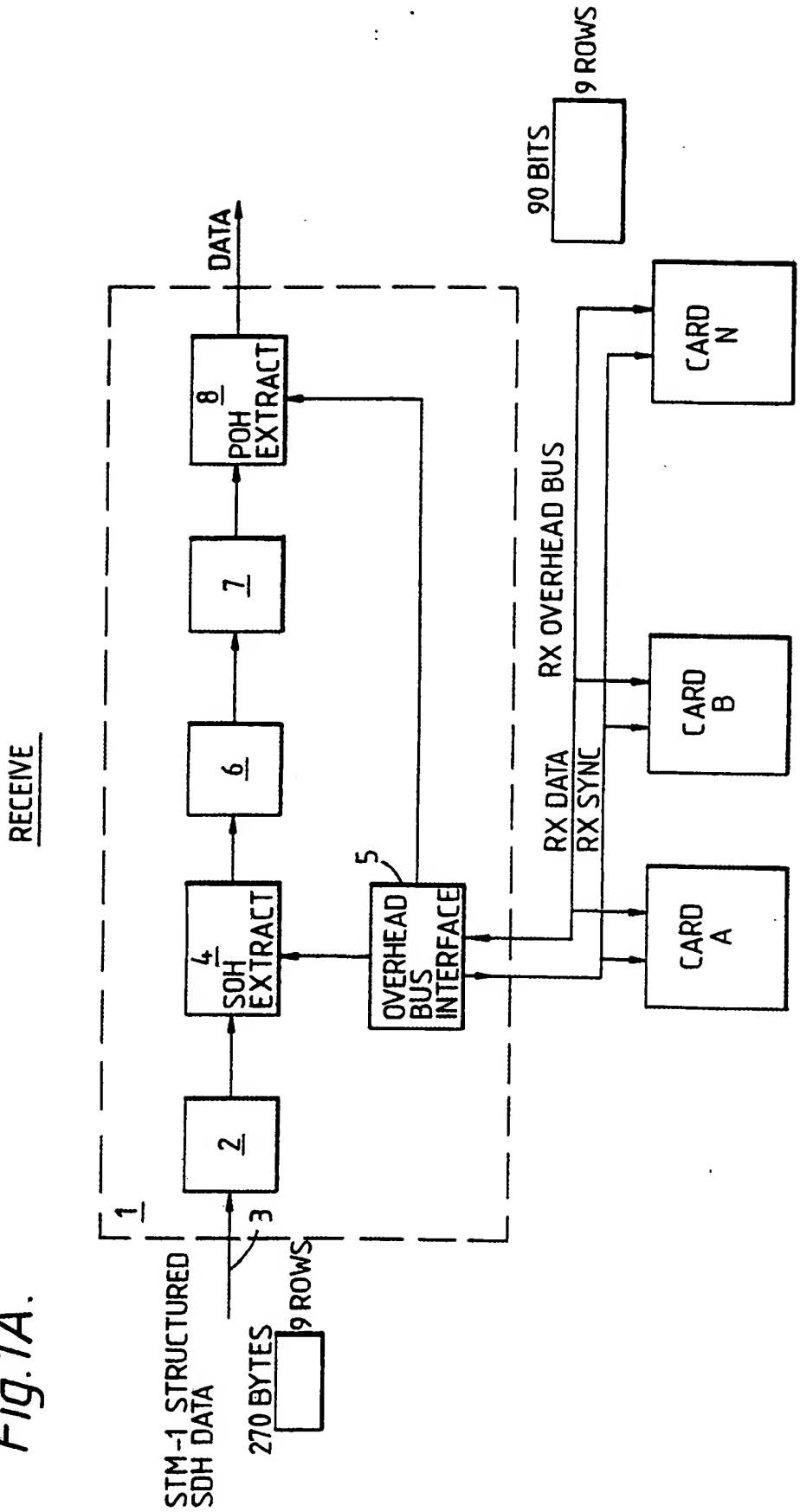
RECEIVE
STM-1 STRUCTURED SDH DATA
270 BYTES
9 ROWS
1
2
3
4 SOH EXTRACT
5 OVERHEAD BUS INTERFACE
6
7
8 POH EXTRACT
DATA
90 BITS
9 ROWS
RX OVERHEAD BUS
RX DATA
RX SYNC
CARD A
CARD B
CARD N

Fig.1A.

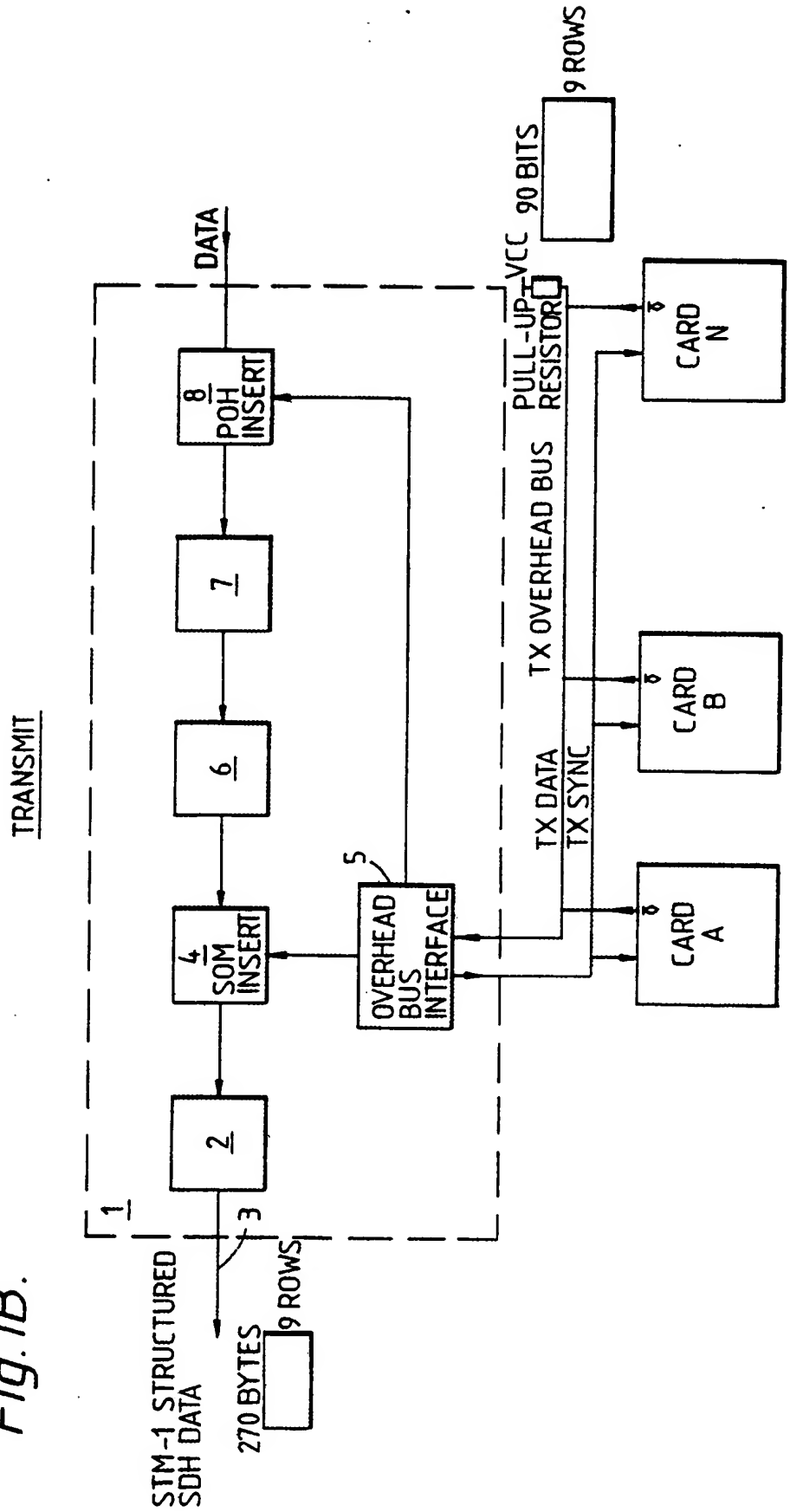
TRANSMIT
DATA
8 POH INSERT
7
6
4 SOM INSERT
2
1
3
5
OVERHEAD BUS INTERFACE
TX DATA
TX SYNC
TX OVERHEAD BUS
PULL-UP RESISTOR
VCC
90 BITS
9 ROWS
CARD N
CARD B
CARD A
STM-1 STRUCTURED SDH DATA
270 BYTES
9 ROWS

Fig. 1B.

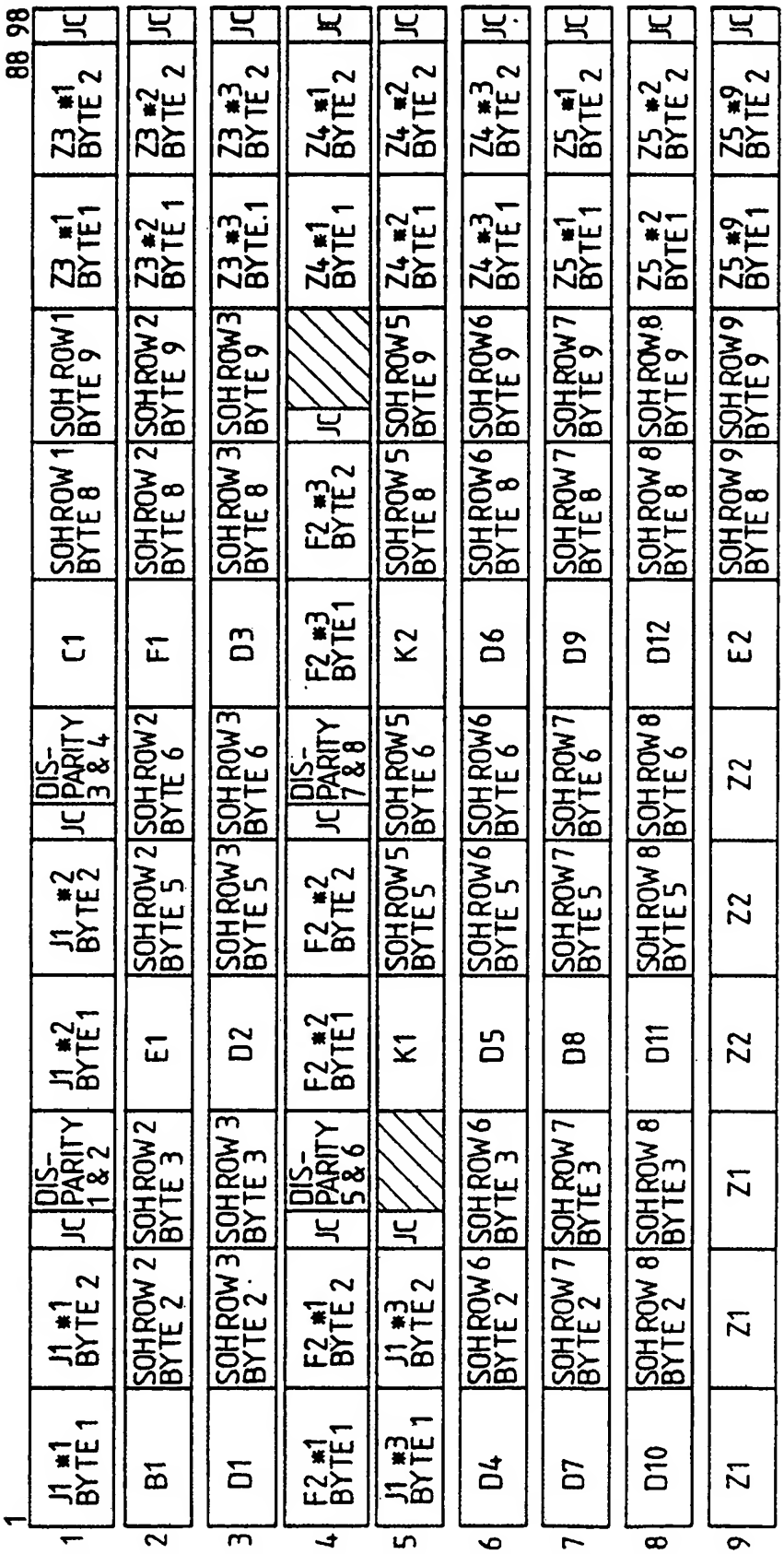
1
88 98
ROW 1
ROW 2
ROW 3
ROW 4
ROW 5
ROW 6
ROW 7
ROW 8
ROW 9
J1 #1 BYTE 1
J1 #1 BYTE 2
JC
DIS-PARITY 1 & 2
J1 #2 BYTE1
J1 #2 BYTE2
JC
DIS-PARITY 3 & 4
C1
SOH ROW 1 BYTE 8
SOH ROW1 BYTE 9
Z3 #1 BYTE1
Z3 #1 BYTE 2
JC
B1
SOH ROW 2 BYTE 2
SOH ROW 2 BYTE 3
E1
SOH ROW 2 BYTE 5
SOH ROW 2 BYTE 6
F1
SOH ROW 2 BYTE 8
SOH ROW2 BYTE 9
Z3 #2 BYTE 1
Z3 #2 BYTE 2
JC
D1
SOH ROW 3 BYTE 2
SOH ROW 3 BYTE 3
D2
SOH ROW 3 BYTE 5
SOH ROW 3 BYTE 6
D3
SOH ROW 3 BYTE 8
SOH ROW3 BYTE 9
Z3 #3 BYTE.1
Z3 #3 BYTE 2
JC
F2 #1 BYTE 1
F2 #1 BYTE 2
JC
DIS-PARITY 5 & 6
F2 #2 BYTE1
F2 #2 BYTE 2
JC
DIS-PARITY 7 & 8
F2 #3 BYTE1
F2 #3 BYTE 2
JC
Z4 #1 BYTE 1
Z4 #1 BYTE 2
JC
J1 #3 BYTE 1
J1 #3 BYTE 2
JC
K1
SOH ROW 5 BYTE 5
SOH ROW 5 BYTE 6
K2
SOH ROW 5 BYTE 8
SOH ROW5 BYTE 9
Z4 #2 BYTE1
Z4 #2 BYTE 2
JC
D4
SOH ROW 6 BYTE 2
SOH ROW 6 BYTE 3
D5
SOH ROW 6 BYTE 5
SOH ROW 6 BYTE 6
D6
SOH ROW 6 BYTE 8
SOH ROW6 BYTE 9
Z4 #3 BYTE 1
Z4 #3 BYTE 2
JC
D7
SOH ROW 7 BYTE 2
SOH ROW 7 BYTE 3
D8
SOH ROW 7 BYTE 5
SOH ROW 7 BYTE 6
D9
SOH ROW 7 BYTE 8
SOH ROW7 BYTE 9
Z5 #1 BYTE1
Z5 #1 BYTE 2
JC
D10
SOH ROW 8 BYTE 2
SOH ROW 8 BYTE 3
D11
SOH ROW 8 BYTE 5
SOH ROW 8 BYTE 6
D12
SOH ROW 8 BYTE 8
SOH ROW8 BYTE 9
Z5 #2 BYTE1
Z5 #2 BYTE 2
JC
Z1
Z1
Z1
Z2
Z2
Z2
E2
SOH ROW 9 BYTE 8
SOH ROW9 BYTE 9
Z5 #9 BYTE1
Z5 #9 BYTE 2
JC
JC
C1
C2
1
1
DISPARITY
DP #N
1
DP #N+1
1
CN=JUSTIFICATION CONTROL BIT FOR BYTE N
CN=0 BYTE N = FIXED STUFF (ALL 1'S)
CN=1 BYTE N = DATA
DP=DISPARITY BIT
UNUSED-FIXED STUFF (ALL 1'S)

Fig. 2.

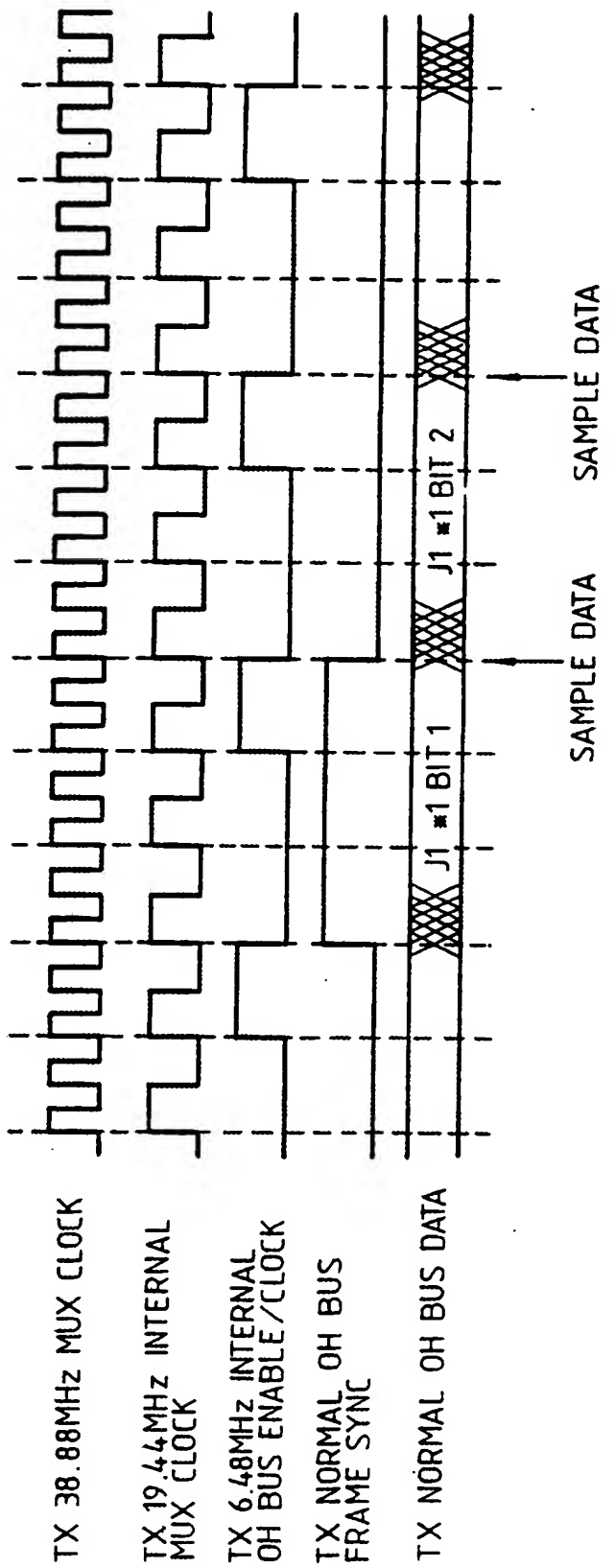
TX 38.88MHz MUX CLOCK
TX 19.44MHz INTERNAL MUX CLOCK
TX 6.48MHz INTERNAL OH BUS ENABLE/CLOCK
TX NORMAL OH BUS FRAME SYNC
TX NORMAL OH BUS DATA
J1 #1 BIT 1
J1 #1 BIT 2
SAMPLE DATA
SAMPLE DATA

Fig. 3.

INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 93/00855

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H04J3/06; H04J3/08; H04J3/14

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H04J

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category[10]	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
A	NACHRICHTENTECHNISCHE BERICHTE no. 9, April 1992, BACKNANG DE pages 30 - 43 T. HARBICH ET AL. 'Synchrone Leitungsausrüstung' see page 31, left column, paragraph 4 see page 31, right column, paragraph 2 see page 31, right column, paragraph 4 see figures 1A,16	1,3-5
A	ICC 91 vol. 2, 23 June 1991, DENVER , US pages 758 - 762 A. TAKASE ET AL. 'LOCAL LOOP SYSTEM EVOLUTION TOWARD B-ISDN WITH AN INTEGRATED MAN/DLC' see page 760, left column, paragraph 3 see page 762, left column, last paragraph; figures 2A,2B	1,3-5

-/--

° Special categories of cited documents :[10]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
28 JULY 1993	09. 08. 93
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	PIEPER T.

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	US,A,4 416 009 (HUFFMAN ET AL.) 15 November 1983 see column 4, line 1 - line 68; figure 5	1
A	US,A,4 156 112 (MORELAND) 22 May 1979 see column 3, line 16 - line 38; figure 1	1,2

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. GB 9300855 SA 73146

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 28/07/93
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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A-4416009	15-11-83	None		
US-A-4156112	22-05-79	CA-A-	1111972	03-11-81
		EP-A,B	0008285	20-02-80
		WO-A-	7900351	28-06-79